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1. A dynamic random access memory having a trench capacitor, said memory comprising:

5 a semiconductor substrate of one conduction type;

a trench formed in said semiconductor substrate;

a first conductive layer formed on the inner surface of said trench except for a region adjacent to the opening portion of said trench;

10 a dielectric layer formed on said first conductive layer exposed in said trench and the surface of said semiconductor substrate;

a second conductive layer filled in said trench through said dielectric layer;

15 said first conductive layer, said dielectric layer, and said second conductive layer constituting a storage capacitor; and

a metal insulator semiconductor transistor formed in said semiconductor substrate, having a source or drain region of the other conduction type which is

20 connected to said second conductive layer.

2. A memory according to claim 1, wherein said second conductive layer is electrically connected with said source or drain region of the <sup>another</sup> other conduction type through a third conductive layer.

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3. A memory according to claim 1, wherein a <sup>distance</sup> predetermined interval is formed between the upper end portion of said first conductive layer and the bottom level of said source or drain layer.

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4. A memory according to claim 3, wherein said predetermined <sup>distance</sup> interval is occupied by an insulator material.

5. A memory according to claim 1, wherein said source or drain region is ~~in~~ adjacent to said second conductive layer through said dielectric layer.

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6. A memory according to claim 1, wherein said

first conductive layer is in contact with said semiconductor substrate in said trench.

7. A memory according to claim 1, wherein said first conductive layer comprises a polycrystalline  
5 silicon.

8. A memory according to claim 1, wherein said dielectric layer has a larger thickness at said surface of said semiconductor substrate than that on said first conductive layer.